RFIC Design and Testing for Wireless Communications

A PragaTI (TI India Technical University) Course
July 18, 21, 22, 2008

Lecture 10: RFIC design for wireless communications

By

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Topics

Monday, July 21, 2008

9:00 – 10:30	Introduction – Semiconductor history, RF characteristics
11:00 – 12:30	Basic Concepts – Linearity, noise figure, dynamic range
2:00 – 3:30	RF front-end design – LNA, mixer
4:00 – 5:30	Frequency synthesizer design I (PLL)

Tuesday, July 22, 2008

9:00 – 10:30	Frequency synthesizer design II (VCO)
11:00 – 12:30	RFIC design for wireless communications
2:00 – 3:30	Analog and mixed signal testing

Survival kit for a good IC designer

- Strong background in analog circuit analysis and designs
- Strong background in digital logic analysis and designs
- Familiarity with EDA tools such as Cadence, Mentor Graphics, Synopsys and ADS IC design tools
- Understanding of device physics
- Knowledge in communication, microwave, DSP and control theories

Analog IC design -- a challenging task

- Analog IC designs deal with multi-dimensional tradeoff of speed, power, gain, linearity, precision, supply, noise, cost, etc.
- Analog circuits are much more sensitive to noise, crosstalk, variation, mismatch and parasitics, due to high speed and precision requirements.
- Modeling and simulation of analog circuits are still problematic and not always accurate. Many hidden problems cannot be discovered in simulation.
- Analog IC design can rarely be automated at high speed. It requires hand-crafted design and layout. Thus, the designer's experience is critical.

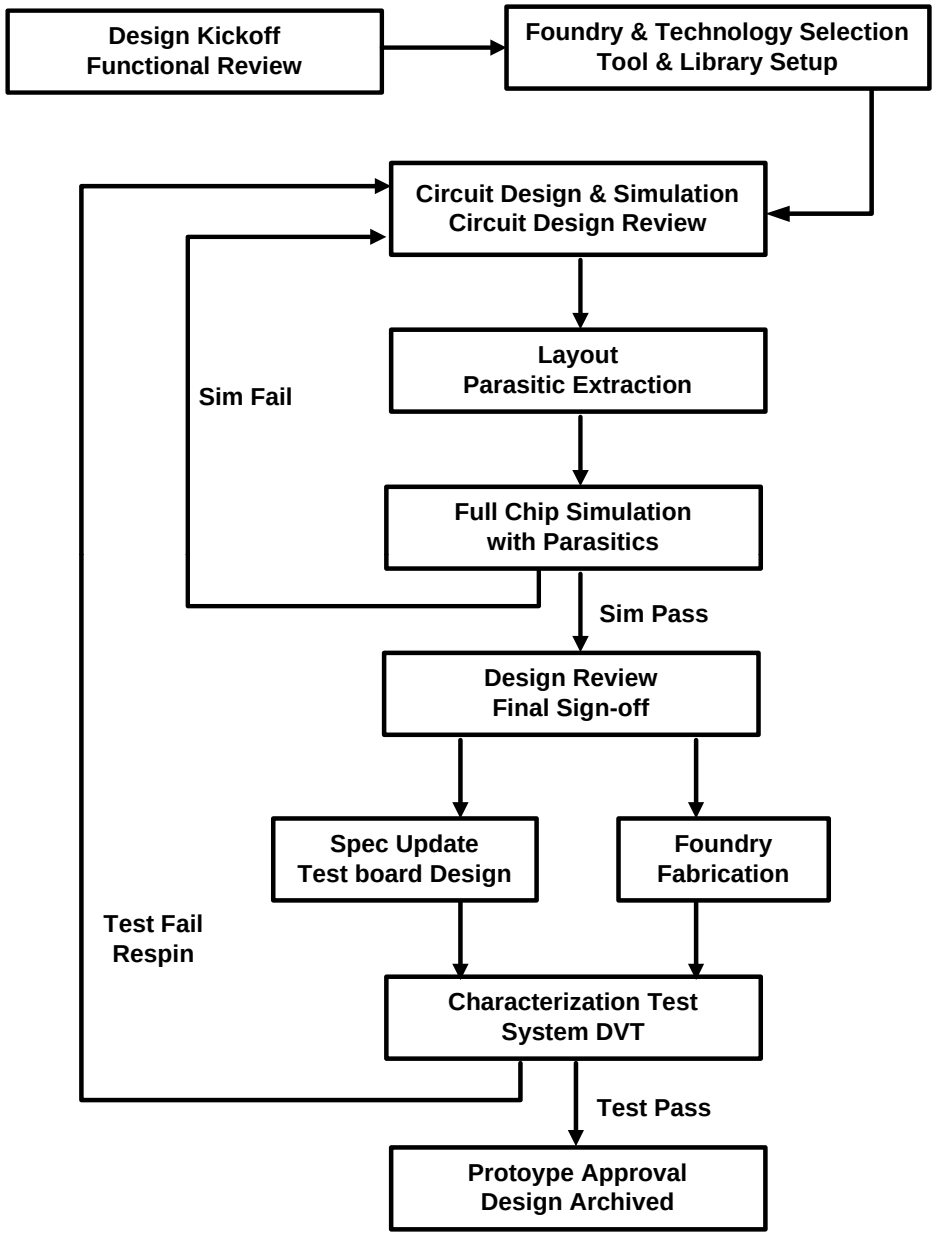
Communication System Concepts

- Noise Analysis – Noise Types, Noise Figure;
- Impedance Matching – to 50 Ohm;
- Linearity Analysis – Intermodulation, Harmonic Distortion, Gain Compression, Spur-free Dynamic Range;
- Frequency Conversion – Spurious Response;
- Receiver/Transmitter Architectures – Homodyne, Heterodyne, Image Reject Receiver;
- Modulation/Demodulation Schemes – AM, FM, BPSK, QPSK, MSK, GMSK, etc.

Communication Circuit Designs

- Device Modeling – BJT (RF Device Model, RF Noise Model), MOS (RF Device Model, RF Noise Model), Passive Elements (Res., Cap. & Ind.)
- LNA Design, VGA Design
- Mixer Design, Image Rejection Mixer
- IQ Modulator Designs, quadrature generation
- RF Circuit Biasing – Bandgap Voltage References, Current References
- Voltage Controlled Oscillators (VCO)
- Phase Locked Loops – Integer PLLs, Fractional-N PLLs, Sigma-delta Modulator, Phase detector, charge pump, MMD
- Integrated filters, Polyphase filters
- Power Amplifiers – Matching, Biasing, Class A, B, C

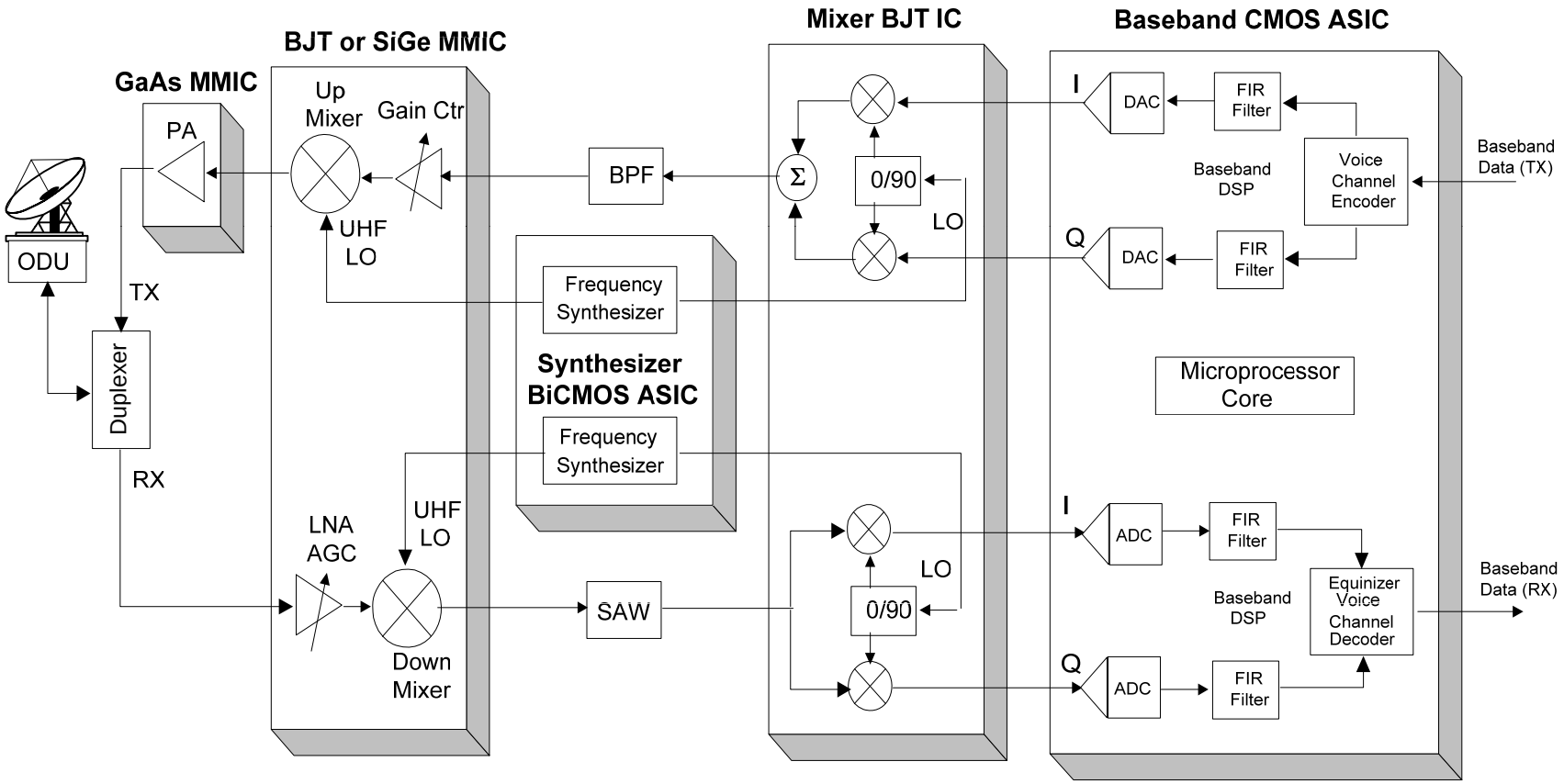
Analog IC Design Flow



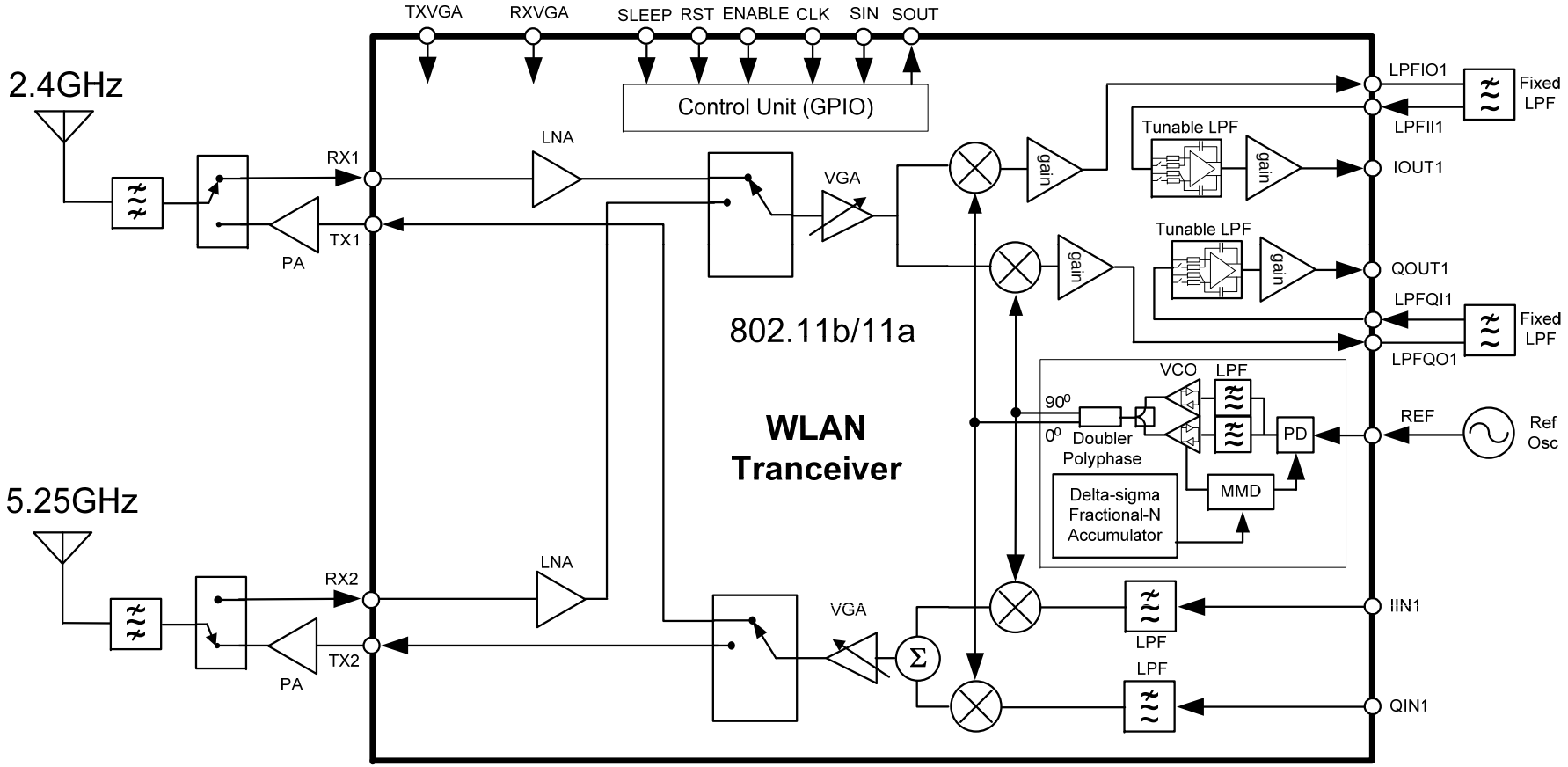
Wireless Standard: WLAN, WIRELESS DATA

STANDARD	BlueTooth	IEEE 802.11		ETS1/BRAN HiperLAN/2 5 GHz
		802.11b 2.4 GHz	802.11a 5.3 GHz	
Mobile Frequency Range	2.402 GHz-2.480 GHz (N. America & Europe 79 Hopping Channel)	2.41 GHz – 2.462 GHz (N. America, 12 channels 1000 mW/MHz Power Allowance)	5.150 GHz – 5.250 GHz (USA U-NII Lower Band, channels 36, 40, 44, 48 2.5 mW/MHz Max Transmit Power)	5.150 GHz – 5.250 GHz, 2.5 mW/Hz 5.250 GHz – 5.350 GHz, 12.5 mW/Hz 5.725 GHz – 5.825 GHz, 50 mW/Hz USA U-NII Band
	2.447 GHz – 2.473 GHz (Spain)			
	2.448 GHz – 2.482 GHz (France)	2.412 GHz – 2.472 GHz (Europe, 12 Channels 100mW/MHz power allowance)	5.250 GHz – 5.350 GHz (USA U-NII Middle Band, channels 52, 56, 60, 64 12.5 mW/MHz Max Transmit Power)	5.150 GHz – 5.350 GHz, 200 mW 5.250 GHz – 5.350 GHz, 1000W 5.725 GHz – 5.825 GHz, 25 mW Europe HiperLAN and ISM
	2.473 GHz – 2.495 GHz (Japan)	2.483 GHz (Japan, 1 cannel 10mW/MHz power allowance)	5.725 GHz – 5.825 GHz (USA U-NII Upper Band, channels 149, 153, 157, 161 50 mW/MHz Max Transmit Power)	5.150 GHz – 5.250 GHz, 100mW Japan (HiSWANa)
Multiple Access	Frequency Hopping	CSMA/CA	CSMA/CA	TDMA
Duplex Method	TDD	TDD	TDD	TDD
Users / Channel	7 active, 200 inactive	127	127	127
Channel Spacing	1 MHz	FHSS: 1 MHz DSSS: 25 MHz	OFDM: 20MHz	OFDM: 20MHz
Modulation	Shaped Binary FM (0.5 Gaussian Filter)	FHSS: GFSX (0.5 Gaussian Filter) DSSS:DBPSK (1 Mb/s) DQPSK (2Mb/s) CCK:QPSK (11 Mb/s)	OFDM: QPSK, QAM (0.5 Gaussian Filter) OFDM: BPSK (5.5 Mb/s) OFDM: 16 QAM (24, 26 Mb/s) OFDM: 64 QAM (54 Mb/s)	OFDM: QPSK, QAM (0.5 Gaussian Filter) OFDM: BPSK (6, 9 Mb/s) OFDM: 16 QAM (24, 36 Mb/s) OFDM: 64 QAM (48, 54 Mb/s)
Channel Bit Rate	1 Mb/s Symbol rate 721 kb/s raw data, 56 kb/s return	1, 2, or 11 Mb/s	12 Mb/s Symbol rate 5.5 – 54 Mb/s	12 Mb/s Symbol rate 6 – 54 Mb/s

IC solution for a typical communication system



RFIC of Dual-band WLAN Transceivers



Wireless RF Transceiver Architectures

- **Superheterodyne**
- **Direction conversion (Zero-IF)**
- **Low IF**
- **Low IF with image rejection mixer**
- **Superheterodyne with walking IF**
- **Direct conversion with $F_{LO}=3/2F_{VCO}$**

Superheterodyne Radio Architecture

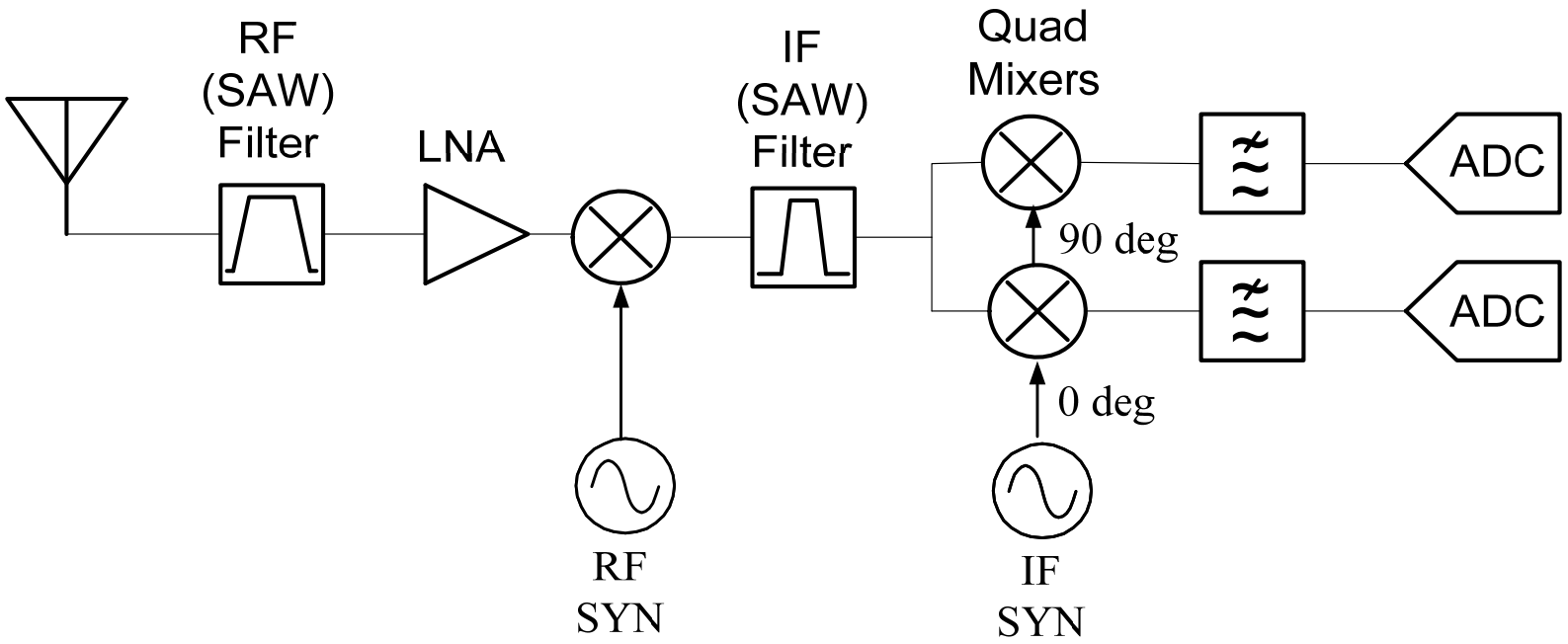
- Advantages:

-- High performance, low power, avoid DC offset

-- Low design risk, easier to design LNA and mixer

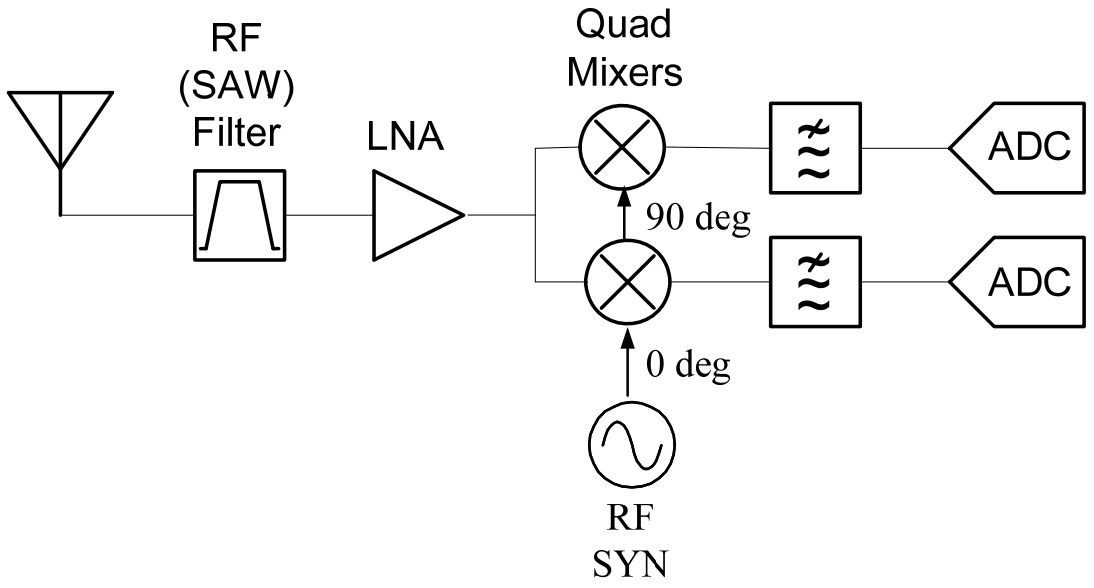
- Disadvantages:

-- High cost, needs two (IF/RF) synthesizers, mixer, filters and S/Hs, external components such as SAW filter



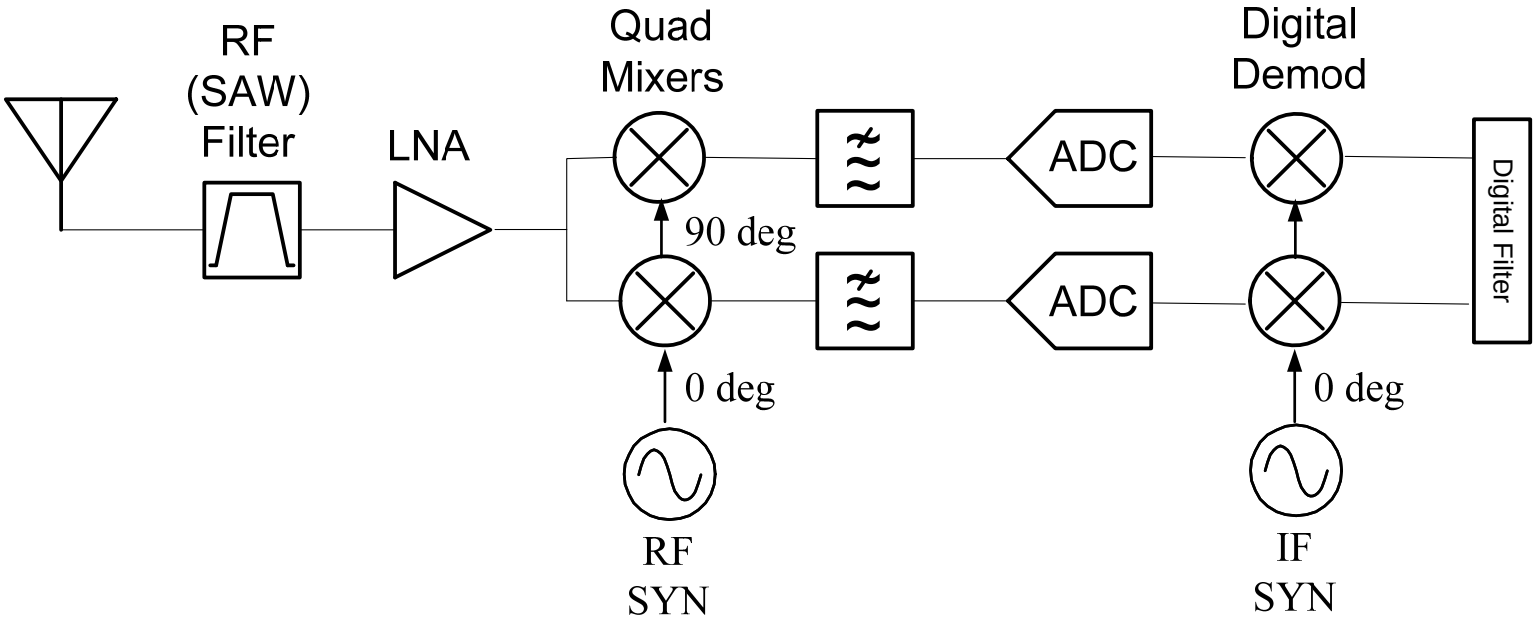
Direct Conversion (Zero-IF) Architecture

- Advantages: Low cost, eliminates IF SAW IF PLL and image filter
- Disadvantages – design challenges:
  - On-board PAs tend to injection lock the VCO
  - Difficult to achieve good I/Q quadrature balance at RF frequencies
  - LO self-mixing causes DC offset that is hard to be compensated
  - AM detection require large 2nd order linearity
  - High power consumption, ~ 10% more than superheterodyne



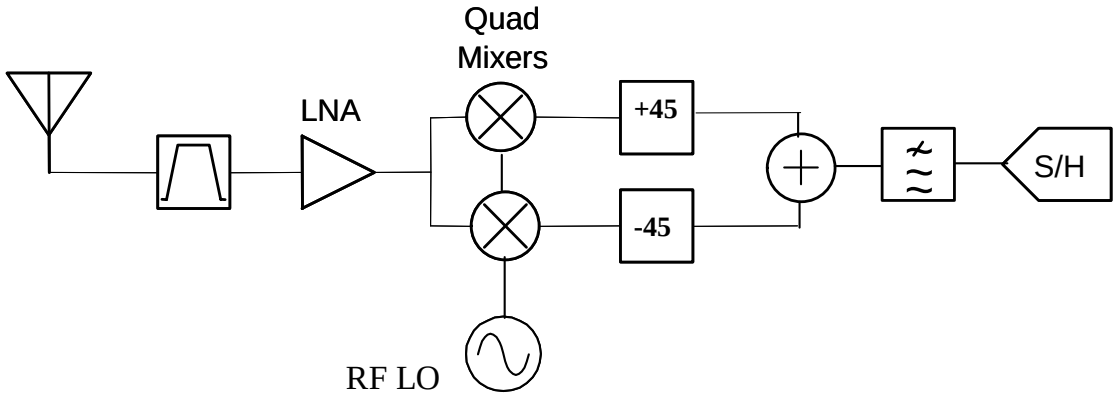
Low IF Radio Architecture

- Advantages:
  - Low cost, eliminates IF SAW, IF PLL and image filter, no DC offset
- Disadvantages:
  - On-board PAs tend to injection lock the VCO
  - Difficult to achieve good I/Q quadrature balance at high LO frequencies
  - High power consumption, ~ 10% more than superheterdyne
  - Requires wider BW lowpass filters and high performance ADC



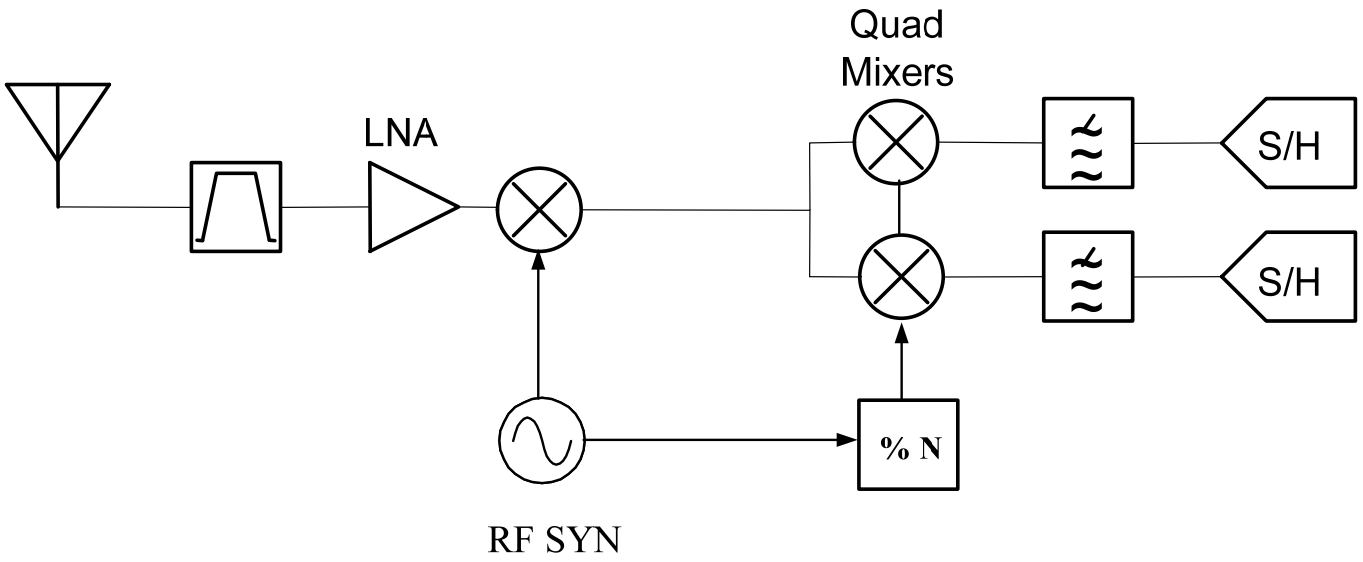
Low IF with image rejection mixer

- Advantages:
  - Low cost, no DC offset
  - Requires only one LPF & S/H
- Disadvantages:
  - On-board PAs tend to injection lock the VCO
  - Difficult to achieve good I/Q quadrature balance at high LO frequencies
  - No DSP I/Q correction possible, requiring very accurate IQ balance in polyphase filters
  - High power consumption, ~ 5-10% more than superheterodyne



Superheterodyne with walking IF

- Advantages:
  - Low cost and high performance, similar risk as superheterodyne, yet save an IF synthesizer
- Disadvantages:
  - Slightly higher power (~5%) than superheterodyne
  - Wider BW for filters



Direct Conversion with $F_{LO}=3/2F_{VCO}$

- Advantages:
  - Avoid pulling, reduce LO-RF interaction
- Disadvantages:
  - Unwanted sideband at ω/3, 5.4GHz/3=1.8GHz (cell phone band)